EMBEDDED SYSTEMS

Comprehensive Guide to 8085 Microprocessor: Architecture, Programming, and Interfacing Strategies

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The evolution of computing technology owes a significant debt to the foundational architectures established in the late 1970s. Among these, the Intel 8085 stands as a monumental pillar in the history of microelectronics and computer engineering. As articulated in the authoritative text **8085 Microprocessor: Programming and Interfacing** by **N.K. Srinath**, this 8-bit microprocessor remains the quintessential learning tool for understanding the intricate relationship between hardware architecture and software execution. This article provides an exhaustive technical analysis of the 8085, exploring its internal structure, instruction set, timing mechanics, and the complex art of peripheral interfacing.

The Significance of 8085 Architecture in Modern Engineering

The 8085 is an 8-bit general-purpose microprocessor capable of addressing 64 KB of memory. While modern processors operate in the gigahertz range with 64-bit word lengths, the 8085 provides a transparent view of the fundamental **Von Neumann architecture**. It integrates a central processing unit (CPU), an arithmetic logic unit (ALU), and a control unit, making it an ideal pedagogical model for undergraduate engineering students in computer science and electronics.

The importance of studying the 8085, as emphasized by N.K. Srinath, lies in its simplicity and the clarity with which it demonstrates **bus cycles**, **interrupt structures**, and **instruction decoding**. Mastering these concepts is essential for any engineer looking to specialize in embedded systems, SoC (System on Chip) design, or firmware development.

Core Technical Specifications

Before diving into the functional blocks, it is essential to understand the basic hardware parameters of the 8085:

- Data Bus: 8-bit wide, used for transferring data between the CPU, memory, and I/O devices.
- Address Bus: 16-bit wide, allowing for a total of 216 (65,536) unique memory locations.
- Clock Speed: Typically operates at 3 MHz, with an internal clock frequency that is half the crystal frequency.
- Power Supply: Requires a single +5V DC supply, a significant improvement over its predecessor, the 8080, which required multiple voltage levels.

Internal Architecture and Register Organization

The internal architecture of the 8085 is a masterpiece of logical organization. It consists of the Register Array, the ALU, and the Instruction Decoder/Machine Cycle Encoder.

The Register Array

The 8085 features a set of 8-bit registers that can be used independently or in pairs to handle 16-bit data. These registers are critical for minimizing memory access time, as operations on registers are significantly faster than operations on memory.

- Accumulator (A): The primary 8-bit register used for all arithmetic and logical operations. The result of an ALU operation is almost always stored here.

- General Purpose Registers (B, C, D, E, H, L): These can be used as six 8-bit registers or as three 16-bit register pairs (BC, DE, HL). The HL pair is particularly important as it serves as a memory pointer in many instructions.
- Program Counter (PC): A 16-bit register that holds the address of the next instruction to be executed.
- Stack Pointer (SP): A 16-bit register that points to the current top of the stack in RAM.

The Flag Register (Status Word)

The 8-bit flag register contains five flip-flops that indicate the status of the ALU after an operation. These flags are vital for conditional branching logic:

1. Sign Flag (S): Set if the result is negative (MSB is 1).
2. Zero Flag (Z): Set if the result is zero.
3. Auxiliary Carry Flag (AC): Used for BCD (Binary Coded Decimal) arithmetic.
4. Parity Flag (P): Set if the result contains an even number of 1s.
5. Carry Flag (CY): Set if an arithmetic operation results in a carry-out or a borrow.

The 8085 Instruction Set: A Taxonomy

Programming the 8085 involves writing **Assembly Language**code, which is then converted into machine-readable hex codes. The instruction set can be categorized into five functional groups.

1. Data Transfer Group

These instructions move data between registers, or between registers and memory. Examples include MOV (Move), MVI (Move Immediate), LXI (Load Register Pair Immediate), and LDA (Load Accumulator Direct).

2. Arithmetic Group

Used for addition, subtraction, increment, and decrement operations. For instance, ADD B adds the contents of register B to the accumulator. The 8085 also supports 16-bit addition through the DAD instruction.

3. Logical Group

This group includes instructions for Boolean operations like ANA (AND), ORA (OR), XRA (XOR), and CMP (Compare). It also includes RLC (Rotate Left) and RRC (Rotate Right) for bit manipulation.

4. Branch Control Group

These instructions allow the program to change its sequence, either unconditionally (JMP, CALL, RET) or conditionally based on the flag register (JZ - Jump if Zero, JNC - Jump if No Carry).

5. Machine Control Group

Instructions in this group control the processor's state, such as HLT (Halt), NOP (No Operation), and instructions for interrupt management like EI (Enable Interrupt) and DI (Disable Interrupt).

Summary Table: Common 8085 Instructions

Opcode	Operand	Description	Addressing Mode
MOV	Rd, Rs	Copy data from Rs to Rd	Register
MVI	Rd, Data	Load 8-bit data into Rd	Immediate
LXI	Rp, 16-bit	Load 16-bit data into Rp pair	Immediate
ADD	M	Add memory content to Accumulator	Register Indirect
STA	Address	Store Accumulator to Memory	Direct

Addressing Modes: The Mechanics of Data Access

The 8085 employs five different addressing modes to determine the location of the operand. Efficiency in programming often depends on choosing the correct mode.

- Immediate Addressing: The data is part of the instruction itself (e.g., MVI A, 05H).
- Register Addressing: The operand is located in a general-purpose register (e.g., MOV A, B).
- Direct Addressing: The 16-bit address of the data is specified in the instruction (e.g., LDA 2000H).
- Indirect Addressing: The address of the data is held in a register pair, usually HL (e.g., MOV A, M).
- Implied Addressing: The operand is hidden within the opcode itself (e.g., CMA - Complement Accumulator).

Timing Diagrams and Machine Cycles

To understand the execution of an instruction, one must analyze the **Timing Diagram**. Every instruction execution consists of one or more **Machine Cycles**, and each machine cycle consists of several **T-states** (clock periods).

Types of Machine Cycles

1. Opcode Fetch: The CPU fetches the operation code from memory. This usually takes 4 T-states.
2. Memory Read: Reading data from memory (3 T-states).
3. Memory Write: Writing data to memory (3 T-states).
4. I/O Read/Write: Communicating with peripheral devices (3 T-states each).

De-multiplexing the Bus: One of the unique features of the 8085 is its multiplexed Address/Data bus (AD0-AD7). This was done to reduce pin count. To separate the lower 8 bits of the address from the data, an external latch (like the 74LS373) is used, triggered by the **ALE (Address Latch Enable)** signal provided by the 8085.

Interrupt Structure of the 8085

Interrupts are signals sent by external devices to the microprocessor, requesting immediate attention. The 8085 manages these requests through a sophisticated priority logic.

Hardware Interrupts

Interrupt Name	Priority	Trigger Type	Vector Address	Maskable
TRAP	1 (Highest)	Edge and Level	0024H	No
RST 7.5	2	Edge	003CH	Yes
RST 6.5	3	Level	0034H	Yes
RST 5.5	4	Level	002CH	Yes
INTR	5 (Lowest)	Level	External	Yes

The **TRAP**interrupt is unique because it is non-maskable, meaning it cannot be disabled by the programmer. It is reserved for critical events like power failures or emergency system shutdowns.

Peripheral Interfacing: Expanding the Ecosystem

A microprocessor is useless without the ability to communicate with the outside world. Interfacing involves connecting the 8085 to memory (RAM/ROM) and I/O devices (Keyboards, Displays, Sensors).

Memory Interfacing and Address Decoding

Because the 8085 has a 16-bit address bus, it can access 64KB of memory. To connect multiple memory chips, **address decoding** is required. A typical decoder, such as the **74LS138**(3-to-8 line decoder), uses the higher-order address bits to enable specific chips, ensuring no two chips attempt to drive the data bus simultaneously.

Programmable Peripheral Interface (8255)

As discussed extensively in Srinath's technical literature, the **Intel 8255 PPI**is the most common chip used for interfacing. It provides 24 I/O pins which can be configured in various modes:

- Mode 0: Basic I/O (Simple input or output).
- Mode 1: Strobed I/O (Handshaking signals for data transfer).
- Mode 2: Bidirectional Bus (Used for communication with other processors).

Comparison: Memory Mapped I/O vs. I/O Mapped I/O

Feature	Memory Mapped I/O	I/O Mapped I/O (Isolated)
Address Space	Shared with 64KB memory	Separate 256 addresses
Control Signals	MEMR / MEMW	IOR / IOW
Instructions Used	Any (MOV, LDA, STA, etc.)	IN and OUT only
Hardware Complexity	Higher decoding complexity	Simpler decoding

Practical Implementation: Building a Step-by-Step Delay Routine

In real-world applications, such as controlling a stepper motor or blinking an LED, time delays are necessary. Since the 8085 executes instructions at a fixed clock speed, we can calculate the exact time taken by a loop.

The Logic of a Delay Loop

A typical delay routine uses a register (e.g., C) loaded with a count, which is then decremented until it reaches zero. The calculation for the delay is:

Total Delay = (Count × T-states of loop instructions) × Clock Period

Sample Assembly Code (Time Delay)

```
LXI B, FFFFH  ; Load BC with max value (10 T-states)
LOOP: DCX B     ; Decrement BC pair (6 T-states)
MOV A, C        ; Move C to A (4 T-states)
ORA B           ; OR A with B to check if BC=0 (4 T-states)
JNZ LOOP        ; Jump to LOOP if not zero (10/7 T-states)
RET             ; Return (10 T-states)
```

By calculating the total T-states and multiplying by the clock period (e.g., 333ns for a 3MHz clock), engineers can achieve precise timing control for hardware synchronization.

Troubleshooting and Debugging in 8085 Systems

Debugging microprocessor-based systems requires a combination of logical analysis and hardware monitoring tools like logic analyzers or oscilloscopes. Common failure modes include:

1. Bus Contention: Occurs when two devices attempt to output data to the bus at the same time. This is usually a result of faulty address decoding logic.
2. Stack Overflow: If PUSH and CALL instructions are used excessively without corresponding POP or RET, the stack may grow into the program memory area, causing unpredictable behavior.
3. Timing Violations: When interfacing with slower memory chips, the 8085 might complete a read cycle before the memory can stabilize its data. This is solved by using the READY pin to insert Wait States.

Summary and Broader Implications for Computing

The study of the 8085 microprocessor, as guided by the structured approach of N.K. Srinath, provides more than

just historical context; it offers a rigorous framework for understanding all digital computing systems. The concepts of registers, ALU operations, bus timing, and interrupt handling are universal. Even in modern high-performance computing, these fundamental blocks exist, albeit at a much larger scale and complexity.

By mastering the 8085, engineers develop an intuitive sense of how software interacts with hardware at the most granular level. This knowledge is indispensable for optimizing code for performance, troubleshooting hardware-firmware conflicts, and designing efficient embedded solutions. Whether used in industrial controllers, automotive systems, or as a stepping stone to 16-bit and 32-bit architectures, the 8085 remains a vital component of a comprehensive technical education in the 21st century.

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